REMARKS

In accordance with the foregoing, claims 1, 4-5, 7-10, 12-16, 18-21, 24-25, 27-30, 33-34, 36-39, and 41 are amended. No new matter is being presented, and approval and entry are respectfully requested.

Claims 1-41 are pending and under consideration. Reconsideration is respectfully requested.

ENTRY OF AMENDMENT UNDER 37 CFR §1.116

Applicant requests entry of this Rule 116 Response because it is believed that the amendment of claims 1, 4-5, 7-10, 12-16, 18-21, 24-25, 27-30, 33-34, 36-39, and 41 puts this application into condition for allowance and should not entail any further search by the Examiner since no new features are being added or no new issues are being raised.

Claims 1, 4-5, 7-10, 12-16, 18-21, 24-25, 27-30, 33-34, 36-39, and 41 are amended to replace the phrase "hardware resource data" with the phrase --information about a hardware resource--. Support for the amendment is found, for example, in paragraphs [0050], [0051], [0054], [0055], and [0057]-[0060] of the specification.

Items 3 and 5: Objection To Claims 1- 41 Because Of Informalities And Rejection Of Claims 1-41 Under 35 U.S.C. §112, first paragraph

In item 3, pages 2-9 of the Office Action, the Examiner objects to claims 1 - 41 because of informalities and in item 5, pages 10-17 of the Office Action, the Examiner rejects claims 1-41 under 35 U.S.C. §112, first paragraph as containing subject matter that was not described in the specification since the phrase "hardware resource data" was not used in the original patent application.

Claims 1, 4-5, 7-10, 12-16, 18-21, 24-25, 27-30, 33-34, 36-39, and 41, all as amended herein, replace the phrase "hardware resource data" with the phrase --information about a hardware resource--.

Applicants submit that the Examiner continues to err in his interpretation of the present invention and in support of the rejection by seemingly interpreting lines of the specification in isolation and not as a whole.

Applicants respectfully point out to the Examiner that the feature "information about a hardware resource" is literally used in paragraph [0051], for example, and as understood by one of ordinary skill in the art could not be otherwise interpreted. In addition, Applicants point out to the Examiner that paragraph [0051] of the specification specifically defines the use of "resource 14" as signifying "information about a hardware resource."

Further, although paragraph numbering refers to the substitute specification filed on May 10, 2005, Applicants point out to the Examiner that the language --information about a hardware resource-- is unchanged from the "original" specification filed on September 28, 2001.

In support of the amendments, Applicants bring to the Examiner's attention the respective support in the specification for the recited features. In particular, those features including "information about a hardware resource" (resource 14) in paragraphs [0050], [0051], [0054], [0055], and [0057]-[0060], etc. of the specification.

As an example, the feature "requesting a resource in which thread manager, which controls threads each forming an execution unit of a program, makes a request for information about a hardware resource" is supported by paragraph [0064] of the specification which discusses:

> When entering the "execution condition", the thread 13 makes a request to the resource manager 12 for securing the resource 14 (that is, information about a hardware source) needed for the first "method"

(emphasis added).

Summary

Applicants submit that claims 1-41 comply with 35 U.S.C. §112, first paragraph and request the objection and rejection by withdrawn.

Items 8-20: Rejection Of Claims 1-41 under 35 U.S.C. §103(a)

In items 8-20, pages 18-38 of the Office Action, the Examiner rejects claims 1-41 under 35 U.S.C. §103(a) as being unpatentable over Chen (U.S.P. 6,466,898) in view of combinations of Dearth et al. (U.S. P. 6,345,242), Dearth et al. (U.S.P. 5,812,824), Hollander (U.S.P. 6,347,388), Kinzelman et al. (U.S. P. 5,594,741), De Yong et al. (U.S.P. 5,355,435), Thekkath et al. (U.S.P. 6,490,642), Markov (U.S. P. 6,314,552), Kasuya (U.S.P. 6,077,304), Furuichi (U.S.P. 5,437,037), and Levy et al. (U.S.P. 6,092,175).

Applicants submit that the Examiner continues to err in his interpretation of the present invention and in support of the rejection by seemingly interpreting each feature of the claims in isolation and not each claim as a whole.

The rejection is traversed. Claim 1, for example, recites a method of simulating an operation of a logical unit, including:

(1) "requesting a resource in which a thread manager . . . makes a request for information about a hardware resource relating to a hardware resource needed for execution of each of threads representative of a series of functions required until the operation of said logical unit reaches completion according to a design specification of said logical unit, to a resource manager which manages said information about the hardware resource" and

(2) "allocating a resource in which said resource manager allocates said information about a hardware resource meeting said request to said thread in accordance with a rule prescribed in advance" and

(3) "controlling a thread in which said thread manager controls an execution state of said thread in accordance with a result of the allocation made by said resource manager, said thread manager and said resource manager executing said requesting, allocating," and

(4) "controlling repeatedly in cooperation with each other until the execution of said thread reaches completion while dynamically allocating information about a hardware resource relating to necessary hardware resources to the thread by said resource manager every time the generated thread is executed simulating the operation of said logical unit to be conducted up to the completion."

Applicants submit none of the cited art, alone or in combination teach features recited by each of the independent claims.

In particular, none of the cited art teach such a "requesting a resource in which a thread manager, which controls threads each forming an execution unit of a program, makes a request for information about a hardware resource (emphasis added)."

Further, none of the cited art, alone or in combination, teach a simulation using information relating to necessary hardware resources, as recited in each of the independent claims.

By contrast, Levy does not teach a technique of a simulation of a logical unit but rather renaming of actual registers.

By contrast, Dearth '242 merely teaches:

> each of tests 120A-C (FIG. 1), which is to carry out transactions with a simulated circuit, e.g., a circuit simulated by simulation systems 140A-C collectively, through a hub 130 is associated with a respective local synchronization thread ("LST") of hub 130. Each LST acts as a synchronization agent for a respective test and represents the synchronization state of the respective test.

(See, for example, col. 5, starting at line 5).

Further, in contrast, Dearth '824 merely teaches):

> reserving of a device of a simulated circuit, the test prevents reservation of the device by other tests and can therefore interact with the device without interference with the interaction by another test.

(See, for example, col., 5, lines 5-10).

That is, the simulations taught by Dearth '242 and Dearth '824 do not teach allocation of information about hardware, but merely a coordination of hardware.

Summary

Since features recited by claims 1-41 are not taught by the cited art and *prima facie* obviousness, is not established, the rejection should be withdrawn and the claims 1-41 allowed.

CONCLUSION

There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

If there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

STAAS & HALSEY LLP

Date: October 10, 2006

By: Paul W Bobowiec

Paul W. Bobowiec
Registration No. 47,431

1201 New York Ave, N.W., 7th Floor
Washington, D.C. 20005
Telephone: (202) 434-1500
Facsimile: (202) 434-1501